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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,909	03/26/2004	Dong-Ho Park	4591-377	5051
20575	7590	06/28/2005	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 1030 SW MORRISON STREET PORTLAND, OR 97205			TRAN, MICHAEL THANH	
			ART UNIT	PAPER NUMBER

2827

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/813,909

Applicant(s)

PARK ET AL.

Examiner

Michael t. Tran

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on March 26, 2004 through November 15, 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-22 is/are allowed.
- 6) ☒ Claim(s) 1,3 and 4 is/are rejected.
- 7) ☒ Claim(s) 2,5 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119


- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 032604.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____


MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated March 26, 2004 through November 15, 2004, claims 1-22 are active in this application.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed March 26, 2004 has been considered.

Claim Objections

4. Claims 2, 5, and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It appears that there should be a semicolon after the third line of claim 7.

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 3 and 4 are rejected under 35 U.S.C 102(b) as being anticipated by Kwon et al. [U.S. Patent #5,768,215].

With respect to claim 1, Kwon et al. disclose, in figures 5, 6, and 11b, a semiconductor memory device comprising: a plurality of first bit lines [1A]; a plurality of second bit lines [1B]; a signal generator circuit [2] structured to produce a flag signal [Rop] notifying a burst [page] read operation; an address generator circuit [12] structured to provide an address in response to the flag signal; a column selection circuit [13] structured to select a part of the plurality of first bit lines in response to the addresses, the first bit lines being connected to the plurality of second bit lines [via st], respectively; and a discharge circuit [3] for discharging [via phi.DCB] voltages from the plurality of second bit lines in response to the flag signal [see figure 11b]. In figure 11b, it is noted that phi.DCB is responsive to signal Rop.

With respect to claim 3, Kwon et al. disclose, in column 2, that the signal generator circuit is structured to produce the flag signal synchronized to a clock signal.

With respect to claim 4, Kwon et al. disclose, in column 1, that the device is applicable to a flash memory.

Allowable Subject Matter

7. Claims 7-22 are allowable over the prior art of record.

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- A signal generator circuit structured to produce the flag signal notifying a next burst read operation after an input of an initial address.
- A discharge circuit comprises: a discharge signal generator structured to produce a discharge signal in response to the flag signal; and a plurality of NMOS transistors respectively connected between the plurality of second bit lines and a ground voltage and controlled by the discharge signal.
- The second bitlines are structured to be discharged before the selecting operation of the column selection circuit.
- A signal generator circuit for generating a flag signal indicating a burst read operation in response to a clock signal and a chip enable signal; and a sense amplification circuit for sensing and amplifying voltages of the selected second bit lines in response to the sense amplification control signals during the burst read operation.

- A discharge circuit for discharging voltages of the plurality of second bit lines in response to the flag signal.
- After the global bit lines are discharged, selecting the local bit lines and the global bit lines in response to the address.
- Sensing the cells located at the new address using the previously discharged one or more bit lines.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.



Michael T. Tran
Art Unit 2827
June 24, 2005

MICHAEL TRAN
PRIMARY EXAMINER